Instruction Manual

Tektronix

TMS855

HyperTransport Bus Software Support

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www.tektronix.com

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Preface

This instruction manual contains specific information about the TMS855 HyperTransport bus software support product and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating bus support products on the logic analyzer, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating bus support products, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of bus support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of logic analyzer online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the target system
- Setting up the logic analyzer to acquire data from the target system
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles Hyper-Transport bus cycles.
- The phrase “information on basic operations” refers to logic analyzer online help or user manual.
- The phrase “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Contacting Tektronix

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Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 6:00 a.m. – 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TMS855 HyperTransport bus support product, and information on connecting your logic analyzer to your target system.

Support Package Description

The TMS855 HyperTransport bus support product acquires, decodes and displays HyperTransport bus cycles. The support product allows you to acquire bus cycles with minimal impact on the normal environment of the system.

The TMS855 HyperTransport bus support product contains four support packages that you can load to handle the various combinations of Upstream and Downstream bus widths and data rates. A description of each support package is listed here.

- HT provides state, timing, triggering, and disassembly support.
- HT_Cal helps adjust the Setup/Hold time.
- HT_Tek provides state, timing, triggering, and disassembly support.
- HT_Tek_Cal helps adjust the Setup/Hold time.

***NOTE**. The support packages HT and HT_Cal differ from HT_Tek, and HT_Tek_Cal, only in the channel assignments. Refer to the section* Symbol and Channel Assignment Tables *on page 3-11 for details.*

Triggering Support. The HT and HT_Tek support packages contain a library of EasyTrigger programs to enable you to quickly trigger on HyperTransport control packets and to filter CRC and NOP packets in real time.

Disassembly Support

The HT and HT_Tek support packages disassemble data acquired from the HyperTransport bus. The features of the disassembler are:

- Decoding all types of HyperTransport Packets.
- Identifying CRC packets using heuristics.
- Supporting disassembly for the 8-bit and 16-bit bus widths for Upstream and Downstream.

- Providing trigger programs for real time filtering of the CRC and NOP packets and to trigger on the HyperTransport packets.
- Color coding for easier identification of the different packet fields.
- Using packet style display for the existing logic analyzer listing window architecture.
- Acquiring Upstream and Downstream 8 and 16-bit buses in one 136-channel TLA7Axx module, when the bus is operating in synchronous mode.

To use this support package efficiently, refer to these documents:

- *HYPERTRANSPORT I/O LINK SPECIFICATION, {HyperTransport Technology Consortium, 22nd November 2002, and Revision 1.05}*
- *HyperTransport Technology, Interface Design Guide, {May, 2002, Revision 1.04}*

Logic Analyzer Software Compatibility

The label on the bus support CD-ROM states which version of logic analyzer software this support package is compatible with.

Logic Analyzer Configuration

The TMS855 HyperTransport bus support product allows a choice of required minimum module configurations. The support package requires one 136-channel TLA7Axx module. You can simultaneously capture different combinations of Upstream and the Downstream buses from the target system assuming that both the Upstream and Downstream clocks are running at the same speed and derived from the same crystal. The different combinations are:

- 8-bit Upstream Bus and 8-bit Downstream Bus
- 16-bit Upstream Bus and 16-bit Downstream Bus
- 8-bit Upstream Bus and 16-bit Downstream Bus
- 16-bit Upstream Bus and 8-bit Downstream Bus

Systems with unique clocks for the Upstream and Downstream buses require two independent 136-channel TLA7Axx modules for simultaneous capture. Module acquisition speed depends on the requirements but is 450 MHz by default for 16-bit and 8-bit buses.

Table 1–1 lists the probe requirements for each of the TMS855 HyperTransport bus support packages.

Table 1–1: Probe requirements for the TMS855 HyperTransport bus support packages

Support package	Upstream and Downstream 16-bit buses	Upstream and Downstream 8-bit buses	Upstream or Downstream 16-bit buses	Upstream or Downstream 8-bit buses
HT, and HT_Cal	Four P6880 probes for TLA7Axx	Two P6880 probes for TLA7Axx	Two P6880 probes for TLA7Axx	One P6880 probe for TLA7Axx
HT_Tek, and HT_Tek_Cal	Four P6880 probes for TLA7Axx	Four P6880 probes for TLA7Axx	Two P6880 probes for TLA7Axx	Two P6880 probes for TLA7Axx

Requirements and Restrictions

Review the electrical specifications in the *Specifications* section on page 4-1 in this manual as they pertain to your target system, as well as the following descriptions of TMS855 HyperTransport bus support product requirements and restrictions.

Hardware Reset

If a hardware reset occurs in your HyperTransport system during an acquisition, the application might acquire an invalid sample.

Clock Rate

The maximum rate for state acquisition is 450 MHz[1].

Setup/Hold Time Adjustments

For correct acquisition, the target system must provide a data valid window of 750 ps. Some target systems may require an adjustment in the Setup/Hold time settings of the logic analyzer to match the data valid window. The HT_Cal and HT_Tek_Cal support packages can be used along with the SHAnalyzer application to find the optimum Setup/Hold time settings for the logic analyzer. For more information, refer to the section *Setup/Hold Time Adjustments* on page 2-19.

Nonintrusive Acquisition

Acquiring HyperTransport bus cycles is nonintrusive to the target system. That is, the TMS855 HyperTransport bus support product does not intercept, modify or present signals back to the target system.

1 Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest bus supported.

Limitations of the Support

The TMS855 HyperTransport bus support product has these limitations.

- If the TMS855 HyperTransport bus support product cannot find the start of a control packet or a CRC packet, it displays a message "Insufficient Data to Disassemble" in the listing window. This usually occurs if there are no data packets or CRC packets in the acquisition. Use the marking options (see page 2–7) to mark the start of a control packet. Once the start of a control packet is known the support package disassembles the HyperTransport packets.
- Since the trigger programs wait until they encounter a Low to High transition in the CTL signal (to identify the start of a control packet), the trigger programs do not trigger the logic analyzer, if there are no transitions on the CTL signal.
- When the CTL signal is asserted, the CAD signals carry either a control packet or a CRC packet. Since the trigger programs cannot differentiate between a CRC packet and a control packet, false triggering may occur. If the logic analyzer triggered on a CRC packet, then try again to trigger on the desired control packet. This happens when CRC and NOP packets are not filtered.

Connecting the Logic Analyzer to a Target System

You can use the channel probes and clock probes, to make the connections between the logic analyzer and your target system.

To connect the probes to the HyperTransport bus signals described in the TMS855 product channel assignment to the target system, follow these steps:

1. Power off your target system. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the target systems, probes, and the logic analyzer module in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the target system.

2. Place the target system on a horizontal, static-free surface.
3. Use Tables 3–17 through 3–34 starting on page 3–19 to connect the channel probes to HyperTransport bus signals in the target system.

Labeling P6880 Probes

The TMS855 HyperTransport bus support product relies on the channel mapping and labeling scheme for the P6880 probe. Apply labels, using the instructions described in the *P6810, P6860, P6880 Logic Analyzer Probes Instruction* manual (Tektronix part number 071-1059-XX).

Operating Basics

Setting Up the Support

This section provides information on how to set up the software support and covers the following topics:

- Installing the support software
- Support package setups
- Clocking options

The information in this section is specific to the operations and functions of the TMS855 HyperTransport bus support product on a Tektronix logic analyzer. Information on basic operations describes general tasks and functions.

Before you acquire and display disassembled data, you need to load the support package and specify the setups for clocking and triggering as described in the logic analyzer online help under “Microprocessor Support”. The support package provides default values for each of these setups, but you can change the setups as needed.

Installing the Support Software

***NOTE**. Before you install any support software, it is recommended you verify that the bus support software is compatible with the logic analyzer software.*

To install the TMS855 HyperTransport bus support product on your Tektronix logic analyzer, follow these steps:

1. Insert the CD-ROM in the CD drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the CD-ROM. A copy of the instruction manual is available on the CD-ROM.

To remove or uninstall software, follow the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

Support Package Setups

The TMS855 HyperTransport bus support product installs four support packages. Each support package offers different clocking and display options.

- HT: This support package has the channel assignment derived from the pin escape defined in *HyperTransport Technology, Interface Design Guide*. Use this support package to acquire and decode the HyperTransport bus cycles. It supports clock rates from DC up to 450 MHz and data rates from DC up to 900 Mb/s. This package supports both Upstream and Downstream 8-bit and 16-bit buses.
- HT_Cal: This support package has the channel assignment derived from the pin escape defined in the *HyperTransport Technology, Interface Design Guide*. Use this support package to optimize the Setup/Hold window of the logic analyzer for the HyperTransport bus. This support package does not decode and display acquired data. It should only be used in conjunction with the SHAnalyzer application.
- HT_Tek: Use this support package to acquire and decode the HyperTransport bus cycles. It supports clock rates from DC up to 450 MHz and data rates from DC up to 900 Mb/s. This package supports both Upstream and Downstream 8-bit and 16-bit buses.
- HT_Tek_Cal: Use this support package to optimize the Setup/Hold window of the logic analyzer for the HyperTransport bus. This support package does not decode and display acquired data. It should only be used in conjunction with the SHAnalyzer application.

Clocking Options

A special custom clocking program is loaded into the module every time you load one of the HT, HT_Tek, HT_Cal, or HT_Tek_Cal support packages from the TMS855 HyperTransport bus support product. Each support package offers different clocking options. You may use the default clocking option or choose an alternate by clicking the “More...” button in the logic analyzer setup window.

HT, HT_Tek, HT_Cal, and HT_Tek_Cal . These four support packages provide eight custom clocking options.

- 1: Upstream UCLK0 (default)
  For a system with common clocks for the Upstream and Downstream buses, choose this option to acquire both Upstream and Downstream cycles using the Upstream CLK0 (U_CLK0). Setup/Hold values for signals on the Upstream and Downstream buses must be referenced to Upstream CLK0 (U_CLK0). Special groups are created to assist in specifying Setup/Hold values.

- 2: Upstream UCLK0 inverted
  Choose this option if the polarity of the Upstream clock is reversed. For a system with common clocks for the Upstream and Downstream buses, choose this option to acquire both Upstream and Downstream cycles using the Upstream CLK0 (U_CLK0). Setup/Hold values for signals on the Upstream and Downstream buses must be referenced to Upstream CLK0 (U_CLK0). Special groups are created to assist in specifying Setup/Hold values.

- 3: Upstream UCLK1
  For a system with common clocks for the Upstream and Downstream buses, choose this option to acquire both Upstream and Downstream cycles using the Upstream CLK1 (U_CLK1). Setup/Hold values for signals on the Upstream and Downstream buses must be referenced to Upstream CLK1 (U_CLK1). Special groups are created to assist in specifying Setup/Hold values.

- 4: Upstream UCLK1 inverted
  Choose this option if the polarity of the Upstream clock is reversed. For a system with common clocks for the Upstream and Downstream buses, choose this option to acquire both Upstream and Downstream cycles using the Upstream CLK1 (U_CLK1). Setup/Hold values for signals on the Upstream and Downstream buses must be referenced to Upstream CLK1 (U_CLK1). Special groups are created to assist in specifying Setup/Hold values.

- 5: Downstream CLK0
  For a system with common clocks for the Upstream and Downstream buses, choose this option to acquire both Upstream and Downstream cycles using

the Downstream CLK0 (D_CLK0). Setup/Hold values for signals on the Upstream and Downstream buses must be referenced to Downstream CLK0 (D_CLK0). Special groups are created to assist in specifying Setup/Hold values.

- 6: Downstream CLK0 inverted
  Choose this option if the polarity of the Downstream clock is reversed. For a system with common clocks for the Upstream and Downstream buses, choose this option to acquire both Upstream and Downstream cycles using the Downstream CLK0 (D_CLK0). Setup/Hold values for signals on the Upstream and Downstream buses must be referenced to Downstream CLK0 (D_CLK0). Special groups are created to assist in specifying Setup/Hold values.

- 7: Downstream CLK1
  For a system with common clocks for the Upstream and Downstream buses, choose this option to acquire both Upstream and Downstream cycles using the Downstream CLK1 (D_CLK1). Setup/Hold values for signals on the Upstream and Downstream buses must be referenced to Downstream CLK1 (D_CLK1). Special groups are created to assist in specifying Setup/Hold values.

- 8: Downstream CLK1 inverted
  Choose this option if the polarity of the Downstream clock is reversed. For a system with common clocks for the Upstream and Downstream buses, choose this option to acquire both Upstream and Downstream cycles using the Downstream CLK1 (D_CLK1). Setup/Hold values for signals on the Upstream and Downstream buses must be referenced to Downstream CLK1 (D_CLK1). Special groups are created to assist in specifying Setup/Hold values.

NOTE. *Systems with unique clocks for the Upstream and Downstream buses require two independent 136-channel modules for simultaneous capture.*

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The following information covers these topics and tasks:

- Acquiring data
- Changing how data is displayed
- Viewing cycle type labels
- Viewing disassembled data in various display formats

Acquiring Data

The TMS855 HyperTransport bus support product installs four different support packages: HT, HT_Tek, HT_Cal, and HT_Tek_Cal.

NOTE. *HT_Cal and HT_Tek_Cal support packages are added for Setup/Hold time adjustments. Use these support packages only when you need to adjust the Setup/Hold time values.*

Once you load a support package, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help.

Changing How Data is Displayed

Common fields and features allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page.

You can make selections unique to the TMS855 HyperTransport bus support product to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

Table 2–1 lists the logic analyzer disassembly display options for the TMS855 HyperTransport bus support product.

Table 2–1: Disassembly display options

Description	Option
Show	All (default) No NOP Packets
Highlight	None (default)
Disassemble Across Gaps	Yes No (default)

Bus Specific Fields

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations).You can change the displayed data in the following ways, for the HT and HT_Tek support packages. The submenu has the titles HT Controls and HT_Tek Controls. Figure 2-1 displays the listing window for the disassembly optons.

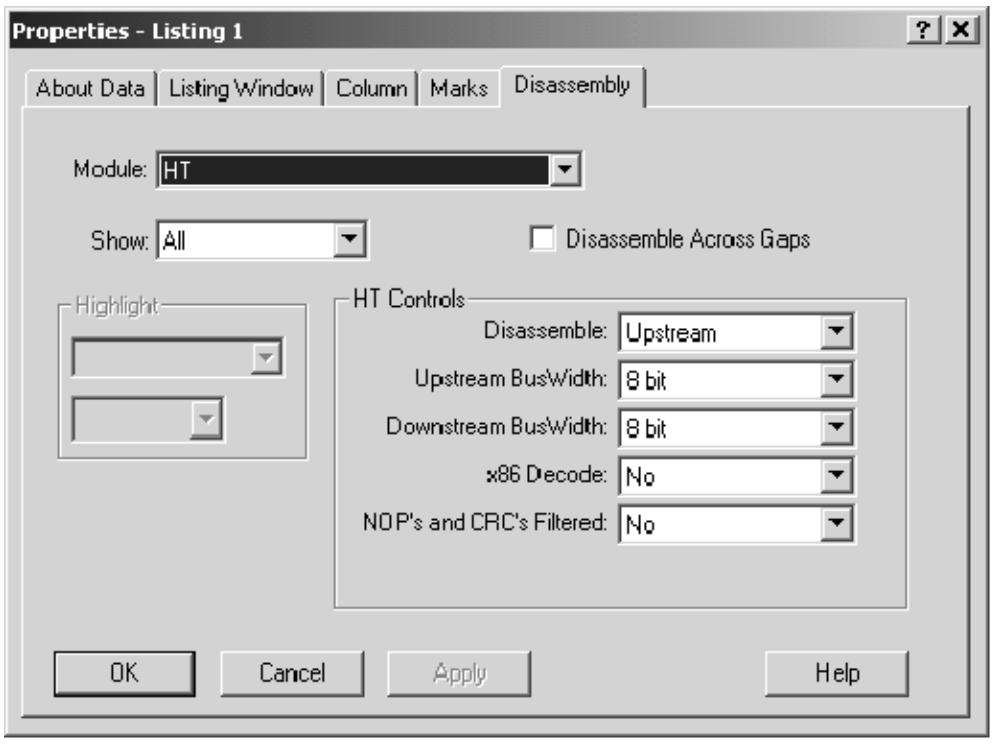


Figure 2–1: Disassembly display options for HT support package

Disassemble. Select one of the two options for the disassembly of either Upstream or Downstream cycles.

Upstream (Default)
Downstream

Upstream Bus Width: Select the Upstream bus width from these options.

8 bit (default)
16 bit
None

Downstream Bus Width: Select the Downstream bus width from these options.

8 bit (default)
16 bit
None

x86 Decode: Two options are available. Set this option to "Yes" to view the x86 packets.

No (default)
Yes

NOPs and CRCs Filtered: Two options are available. Set this option to "Yes" if the CRC and NOP packets are filtered in real time through trigger programs.

No (default)
Yes

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it.

Marks are placed by using the Mark Opcode button. The Mark Opcode button will always be available when disassembly is available. If the sample being marked is not a Control Packet, a note indicating that "An opcode Mark cannot be placed at the selected data sample" will replace the Mark Opcode selections.

When a cycle is marked, the character "»" is displayed immediately to the left of the "HT Frames" or "HT_Tek Frames" column. Cycles can be unmarked by using the "Undo Mark" selection, which will remove the character "»".

Table 2–2 shows the mark selections available on the control packets.

Table 2–2: Mark selections and definitions for HT and HT_Tek support packages

Mark selection	Definition
Control	Marks cycle as start of control packet
Undo Mark	Remove all marks for the current sample

Cycle Type Labels

The HT and HT_Tek support packages decode and display all the individual fields of each packet type. These fields are displayed in different colors.

The control packet names are highlighted in cyan except for Sync Pattern which is highlighted in yellow. Table 2–3 lists the cycle type labels for the HyperTransport control packets.

Table 2–3: Cycle type labels for control packets in HT and HT_Tek support packages

Cycle type labels	Description
NOP Packet	NOP Packet Name
Reserved-HOST	Control packet with a reserved command code
Flush	Flush Packet Name
Write Request	Sized Write Request Packet Name
Read Request	Sized Read Request Packet Name
Reserved-I/O	Control packet with a reserved command code
Read Response	Read Response (RdResponse) Packet Name
Target Done	Target Done (TgtDone) Packet Name
Broadcast Message	Broadcast Message Packet Name
Fence	Fence Packet Name
Atomic Read-Modify-Write Request	Atomic Read-Modify-Write (RMW) Request Packet Name
Sync Pattern	Sync Pattern Packet Name
Interrupt Request	Interrupt Request Packet Name
End of Interrupt	EOI Packet Name
System Management Request-WrSized	System Management Request WrSized Packet Name
System Management Request-Broadcast	System Management Request Broadcast Packet Name

Table 2-3: Cycle type labels for control packets in HT and HT_Tek support packages (Cont.)

Cycle type labels	Description
x86 Interrupt Request	x86 Interrupt Request Packet Name
x86 End of Interrupt	Standard End-of-Interrupt (EOI) Packet Name.
Address Extension	Address Extension
Device Message Request	Device Message Request Packet Name
CRC Transfer	This message is displayed for CRC packets

The data packet label is highlighted in green. Table 2-4 lists the cycle type label for the data packet.

Table 2-4: Cycle type labels for data packets for HT and HT_Tek support packages

Cycle type labels	Description
Data Packet	This message is displayed at the start of a data packet.

Table 2-5 lists the cycle type label for the packet continuation.

Table 2-5: Cycle type labels for packet continuation for HT and HT_Tek support packages

Cycle type Labels	Description
Data Packet Continued...	Data packet continuation. This message is highlighted in green.

Special Messages

This section gives information about the special messages used in the TMS855 HyperTransport bus support product. The disassembler uses special messages to indicate the following significant events. These messages are highlighted in yellow.

Table 2–6 lists the special messages and their descriptions.

Table 2–6: Description of special messages in the display

Special characters	Description
*** Insufficient Data to Disassemble ***	If the TMS855 support software cannot find the start of a control packet or a CRC packet, this message is displayed. This message is also displayed when all the bytes of the control packet are not available for disassembly.

Viewing Disassembled Data

You can view disassembled data for the HT and HT_Tek support packages in two display formats:

All
No NOP Packets

The information on basic operations in the logic analyzer online help describes how to select the disassembly display formats.

***NOTE**. You must set the display format selections in the Disassembly property page for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–5.*

If a channel group is not visible, you must use Add Column or Ctrl+L to make the group visible.

The disassembler displays special characters and strings in the “HT Frames” or “HT_Tek Frames” column to indicate significant events.

Table 2–7 lists these special characters and strings and describes what they represent.

Table 2–7: Description of special characters in the display

Special characters	Description
>	There is insufficient room on the screen to show all available data.
h	The values of the packet fields are displayed in hexadecimal. This character is suffixed with the field value.

All Display Format

This option displays all the information acquired from the HyperTransport bus without suppressing any information. The display consists of HyperTransport packets with all packet fields decoded.

Figure 2–2 shows the disassembly for 8-bit Upstream bus.

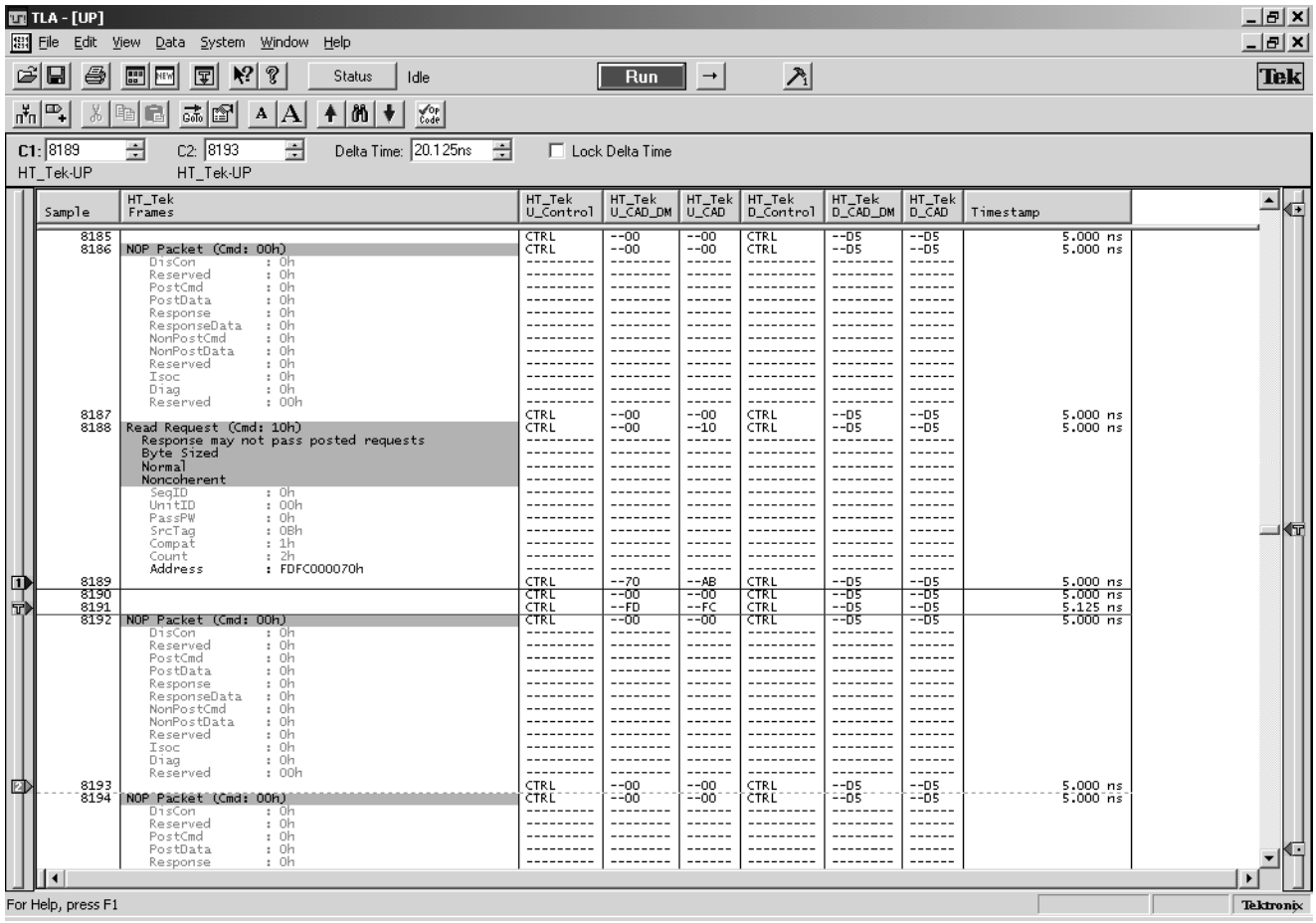


Figure 2–2: Example of All Display format for the HT_Tek support package

Figure 2–3 shows the disassembly for 8-bit Upstream bus with real time filtering of CRC and NOP packets.

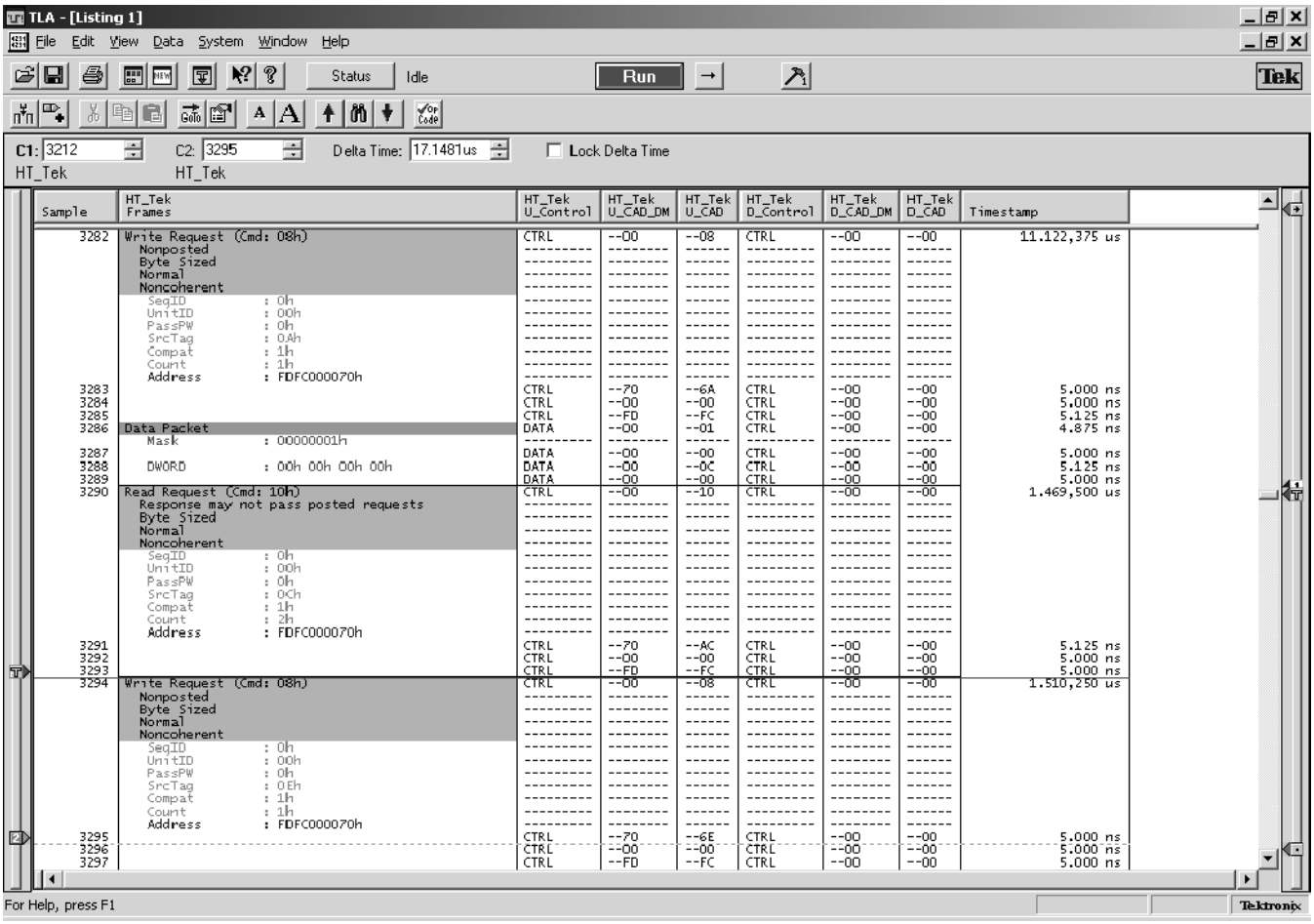


Figure 2–3: Example of All Display format with CRC and NOP packets filtered for the HT_Tek support package

No NOP Packets Display Format

This option displays all packet types with the fields of the packet decoded. The NOP packets are suppressed in this display format.

Figure 2–4 shows the disassembly for 8-bit Upstream bus with Post Process filtering of NOP Packets.

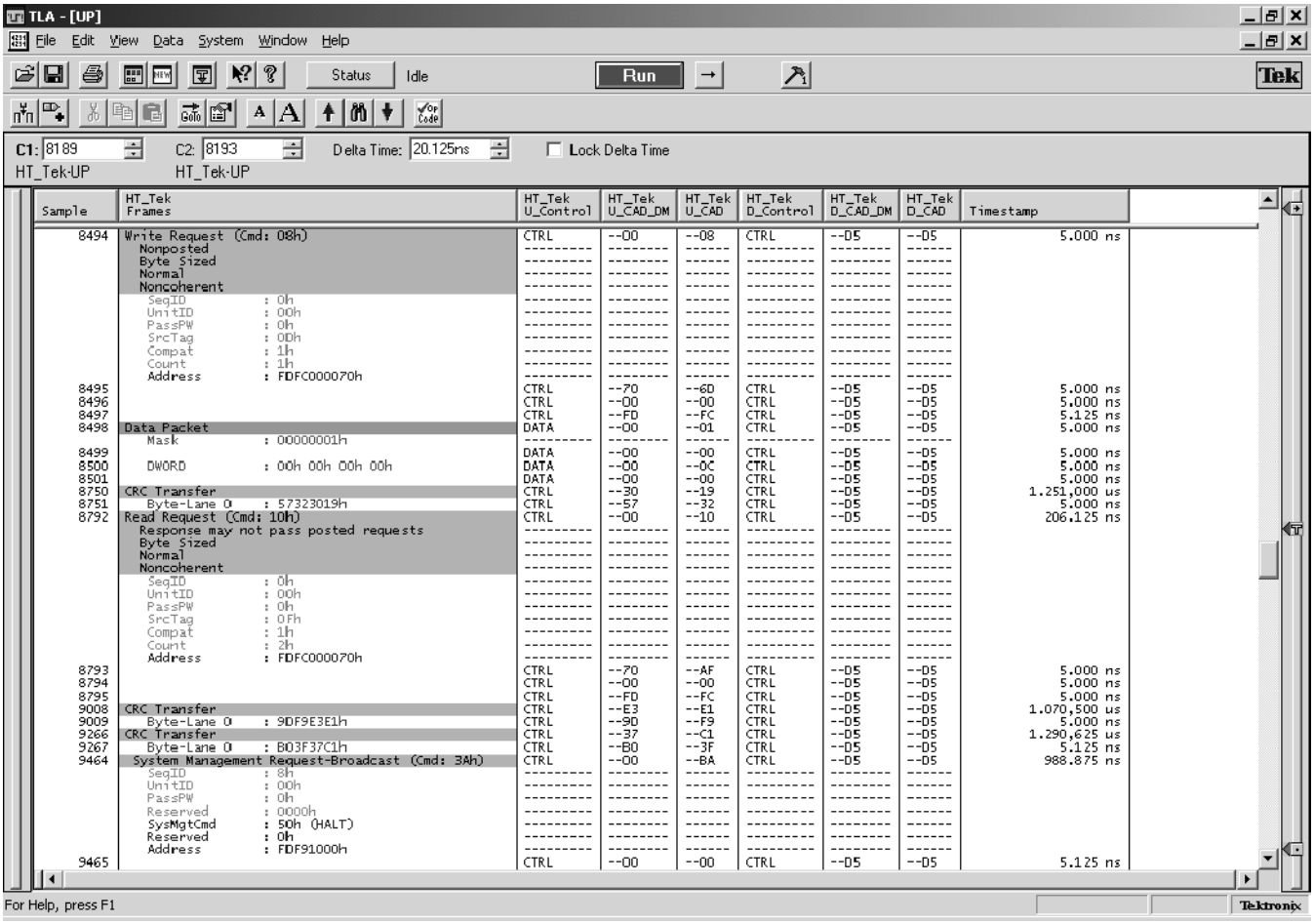


Figure 2–4: Example of No NOP Packets with Post Process filtering in HT_Tek support package

Trigger Programs

This section describes how to load the trigger programs for HT and HT_Tek support packages. The HT and HT_Tek support packages contain a library of EasyTrigger programs enabling you to trigger on the HyperTransport packets and filter CRC and NOP packets in real time.

The TMS855 HyperTransport bus support product installs the trigger programs for each support package in the following paths:

C:\Program Files\TLA700\Supports\HT\EasyTriggers
C:\Program Files\TLA700\Supports\HT_Tek\EasyTriggers

Loading Trigger Programs

To load a trigger program from any of the support packages, follow these steps:

1. Load the support package.
2. From the system window, click the 

Trigger button.

3. Figure 2–5 shows the window that opens.

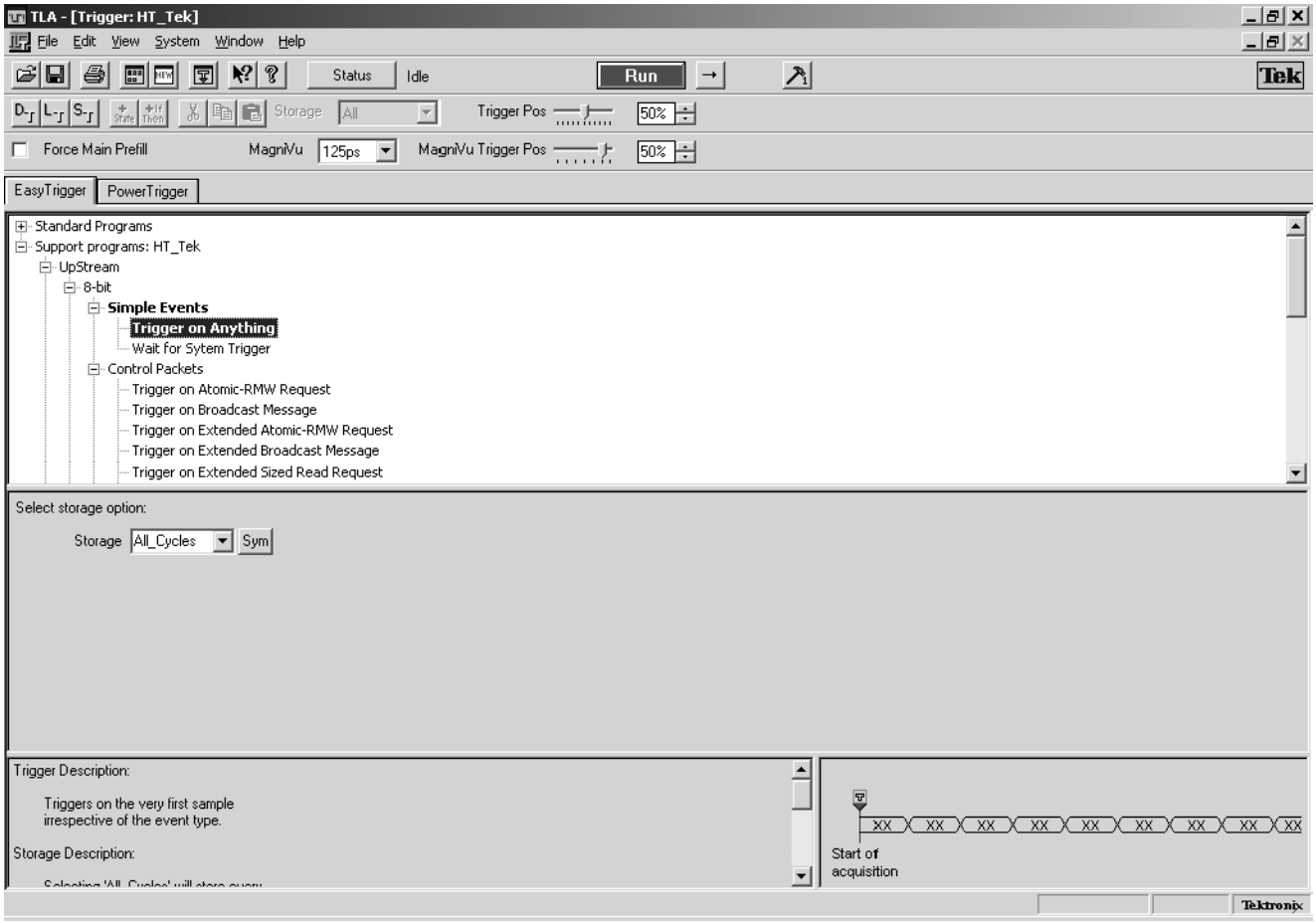


Figure 2–5: Loading trigger programs

4. Scroll through the EasyTriggers to find the trigger programs that you need.
5. Select an EasyTrigger program from the list and fill in the fields.

You are now ready to trigger on the acquired data. For more information on basic operations, refer to the logic analyzer online help and the logic analyzer user manual.

HT and HT_Tek Trigger Programs

The following is a list of EasyTrigger programs for 16-bit and 8-bit wide Upstream and Downstream HyperTransport bus.

Trigger on Anything
Wait for System Trigger
Trigger on Atomic-RMW Request

Trigger on Broadcast Message
Trigger on Device Message Request
Trigger on Extended Atomic–RMW Request
Trigger on Extended Broadcast Message
Trigger on Extended Sized Read Request
Trigger on Extended Sized Write Request
Trigger on Fence Request
Trigger on Flush Request
Trigger on Generic End-Of-Interrupt (EOI)
Trigger on Generic Interrupt
Trigger on NOP
Trigger on Read Response
Trigger on Sized Read Request
Trigger on Sized Write Request
Trigger on Sync Pattern
Trigger on System Management Broadcast Request
Trigger on System Management Write Request
Trigger on Target Done Response
Trigger on x86 End-Of-Interrupt (EOI)
Trigger on x86 Interrupt
Trigger on Data Anywhere in packet
Trigger on Data from Start-of-Packet (SOP)
Trigger on Reserved Command
Trigger on CTL deassertion timeout

Setup/Hold Time Adjustments

Some devices you test may require an adjustment of the setup/hold values in the TLA700 Application. An automated setup/hold analysis application is provided to aid in the selection of the proper setup/hold values. The SHAnalyzer application (SHAnalyzer.exe) and SHAnalyzer help file (SHAnalyzer.chm) are located in the following folders:

C:\Program Files\TLA 700\Supports\HT_Cal
C:\Program Files\TLA 700\Supports\HT_Tek_Cal

To run the SHAnalyzer application on your Tektronix logic analyzer, follow these steps:

1. Start the logic analyzer application and load the appropriate calibration support package, HT_Cal or HT_Tek_Cal.
2. Click the Windows Start button and click Run.
3. Enter the path name (C:\Program Files\TLA 700\Supports\HT_Cal or C:\Program Files\TLA 700\Supports\HT_Tek_Cal) followed by "\SHAnalyzer.exe".
4. Click OK.
5. In the SHAnalyzer application, click the Help button for detailed instructions.

Reference

Channel Group Definitions

This section lists the channel group definitions for the TMS855 HyperTransport bus support product.

Channel Groups

Table 3–1 shows the channel groups for the TMS855 HyperTransport bus support product for the HT and HT_Tek support packages.

Table 3–1: HT and HT_Tek Channel groups

Group name	Display radix
$U_CTL	Off (Calibration group)
$U_CAD0	Off (Calibration group)
$U_CAD1	Off (Calibration group)
$U_CAD2	Off (Calibration group)
$U_CAD3	Off (Calibration group)
$U_CAD4	Off (Calibration group)
$U_CAD5	Off (Calibration group)
$U_CAD6	Off (Calibration group)
$U_CAD7	Off (Calibration group)
$U_CAD8	Off (Calibration group)
$U_CAD9	Off (Calibration group)
$U_CAD10	Off (Calibration group)
$U_CAD11	Off (Calibration group)
$U_CAD12	Off (Calibration group)
$U_CAD13	Off (Calibration group)
$U_CAD14	Off (Calibration group)
$U_CAD15	Off (Calibration group)
$D_CTL	Off (Calibration group)
$D_CAD0	Off (Calibration group)
$D_CAD1	Off (Calibration group)
$D_CAD2	Off (Calibration group)
$D_CAD3	Off (Calibration group)
$D_CAD4	Off (Calibration group)
$D_CAD5	Off (Calibration group)

Table 3-1: HT and HT_Tek Channel groups (Cont.)

Group name	Display radix
$D_CAD6	Off (Calibration group)
$D_CAD7	Off (Calibration group)
$D_CAD8	Off (Calibration group)
$D_CAD9	Off (Calibration group)
$D_CAD10	Off (Calibration group)
$D_CAD11	Off (Calibration group)
$D_CAD12	Off (Calibration group)
$D_CAD13	Off (Calibration group)
$D_CAD14	Off (Calibration group)
$D_CAD15	Off (Calibration group)
HT Frames*	NONE (Disassembly generated text)
HT U_Control*	Symbol (Disassembly generated text)
HT U_CAD_DM*	Hexadecimal
HT U_CAD*	Hexadecimal
HT D_Control*	Symbol (Disassembly generated text)
HT D_CAD_DM*	Hexadecimal
HT D_CAD*	Hexadecimal
HT_Tek Frames**	NONE (Disassembly generated text)
HT_Tek U_Control**	Symbol (Disassembly generated text)
HT_Tek U_CAD_DM**	Hexadecimal
HT_Tek U_CAD**	Hexadecimal
HT_Tek D_Control**	Symbol (Disassembly generated text)
HT_Tek D_CAD_DM**	Hexadecimal
HT_Tek D_CAD**	Hexadecimal
Timestamp	
U_16	Off
D_16	Off
U_8	Off
D_8	Off
zNOP	Off (EasyTrigger group)
U16_Cmd	Off (EasyTrigger group)

* **These groups are displayed only in the HT support package.**

** **These groups are displayed only in the HT_Tek support package.**

Table 3-1: HT and HT_Tek Channel groups (Cont.)

Group name	Display radix
U16_SeqID[3:0]	Off (EasyTrigger group)
U16_PassPW	Off (EasyTrigger group)
U16_UnitID[4:0]	Off (EasyTrigger group)
U16_Count[3:0]	Off (EasyTrigger group)
U16_Compat	Off (EasyTrigger group)
U16_SrcTag[4:0]	Off (EasyTrigger group)
U16_Addr2[7:0]	Off (EasyTrigger group)
U16_Addr3[7:0]	Off (EasyTrigger group)
U16_Addr[39:8]	Off (EasyTrigger group)
U16_Addr[63:40]	Off (EasyTrigger group)
U16_Isoc	Off (EasyTrigger group)
U16_Bridge	Off (EasyTrigger group)
U16_Error	Off (EasyTrigger group)
U16_NXA	Off (EasyTrigger group)
U16_IntrInfo[7:2]	Off (EasyTrigger group)
U16_IntrInfo[31:8]	Off (EasyTrigger group)
U16_Addr[39:32]	Off (EasyTrigger group)
U16_IntrInfo[55:32]	Off (EasyTrigger group)
U16_MT[2:0]	Off (EasyTrigger group)
U16_SysMgtCmd[7:0]	Off (EasyTrigger group)
U16_Addr[39:20]	Off (EasyTrigger group)
U16_MT[3:0]	Off (EasyTrigger group)
U16_Dest	Off (EasyTrigger group)
U16_RQEOI	Off (EasyTrigger group)
U16_Addr[39:24]	Off (EasyTrigger group)
U16_IntrDest[7:0]	Off (EasyTrigger group)
U16_Vector[7:0]	Off (EasyTrigger group)
U16_IntrDest[31:8]	Off (EasyTrigger group)
U16_ResponseData[1:0]	Off (EasyTrigger group)
U16_Response[1:0]	Off (EasyTrigger group)
U16_PostData[1:0]	Off (EasyTrigger group)
U16_PostCmd[1:0]	Off (EasyTrigger group)
U16_Isoc2	Off (EasyTrigger group)
U16_Diag	Off (EasyTrigger group)
U16_NonPostData[1:0]	Off (EasyTrigger group)

Table 3-1: HT and HT_Tek Channel groups (Cont.)

Group name	Display radix
U16_NonPostCmd[1:0]	Off (EasyTrigger group)
U16_DataError	Off (EasyTrigger group)
U16_DestDev	Off (EasyTrigger group)
U16_DestFunc	Off (EasyTrigger group)
U16_DestBus	Off (EasyTrigger group)
U16_Type	Off (EasyTrigger group)
U16_Addr[39:29]	Off (EasyTrigger group)
D16_Cmd	Off (EasyTrigger group)
D16_SeqID[3:0]	Off (EasyTrigger group)
D16_PassPW	Off (EasyTrigger group)
D16_UnitID[4:0]	Off (EasyTrigger group)
D16_Count[3:0]	Off (EasyTrigger group)
D16_Compat	Off (EasyTrigger group)
D16_SrcTag[4:0]	Off (EasyTrigger group)
D16_Addr2[7:0]	Off (EasyTrigger group)
D16_Addr3[7:0]	Off (EasyTrigger group)
D16_Addr[39:8]	Off (EasyTrigger group)
D16_Addr[63:40]	Off (EasyTrigger group)
D16_Isoc	Off (EasyTrigger group)
D16_Bridge	Off (EasyTrigger group)
D16_Error	Off (EasyTrigger group)
D16_NXA	Off (EasyTrigger group)
D16_IntrInfo[7:2]	Off (EasyTrigger group)
D16_IntrInfo[31:8]	Off (EasyTrigger group)
D16_Addr[39:32]	Off (EasyTrigger group)
D16_IntrInfo[55:32]	Off (EasyTrigger group)
D16_MT[2:0]	Off (EasyTrigger group)
D16_SysMgtCmd[7:0]	Off (EasyTrigger group)
D16_Addr[39:20]	Off (EasyTrigger group)
D16_MT[3:0]	Off (EasyTrigger group)
D16_Dest	Off (EasyTrigger group)
D16_RQEOI	Off (EasyTrigger group)
D16_Addr[39:24]	Off (EasyTrigger group)
D16_IntrDest[7:0]	Off (EasyTrigger group)
D16_Vector[7:0]	Off (EasyTrigger group)

Table 3-1: HT and HT_Tek Channel groups (Cont.)

Group name	Display radix
D16_IntrDest[31:8]	Off (EasyTrigger group)
D16_ResponseData[1:0]	Off (EasyTrigger group)
D16_Response[1:0]	Off (EasyTrigger group)
D16_PostData[1:0]	Off (EasyTrigger group)
D16_PostCmd[1:0]	Off (EasyTrigger group)
D16_Isoc2	Off (EasyTrigger group)
D16_Diag	Off (EasyTrigger group)
D16_NonPostData[1:0]	Off (EasyTrigger group)
D16_NonPostCmd[1:0]	Off (EasyTrigger group)
D16_DataError	Off (EasyTrigger group)
D16_DestDev	Off (EasyTrigger group)
D16_DestFunc	Off (EasyTrigger group)
D16_DestBus	Off (EasyTrigger group)
D16_Type	Off (EasyTrigger group)
D16_Addr[39:29]	Off (EasyTrigger group)
U8_Cmd	Off (EasyTrigger group)
U8_SeqID[3:0]	Off (EasyTrigger group)
U8_PassPW	Off (EasyTrigger group)
U8_UnitID[4:0]	Off (EasyTrigger group)
U8_Count[3:0]	Off (EasyTrigger group)
U8_Compat	Off (EasyTrigger group)
U8_SrcTag[4:0]	Off (EasyTrigger group)
U8_Addr2[7:0]	Off (EasyTrigger group)
U8_Addr3[7:0]	Off (EasyTrigger group)
U8_Addr[23:8]	Off (EasyTrigger group)
U8_Addr[39:24]	Off (EasyTrigger group)
U8_Addr[47:40]	Off (EasyTrigger group)
U8_Addr[63:48]	Off (EasyTrigger group)
U8_Isoc	Off (EasyTrigger group)
U8_Bridge	Off (EasyTrigger group)
U8_Error	Off (EasyTrigger group)
U8_NXA	Off (EasyTrigger group)
U8_IntrInfo[7:2]	Off (EasyTrigger group)
U8_IntrInfo[23:8]	Off (EasyTrigger group)
U8_IntrInfo[31:24]	Off (EasyTrigger group)

Table 3-1: HT and HT_Tek Channel groups (Cont.)

Group name	Display radix
U8_IntrInfo[47:32]	Off (EasyTrigger group)
U8_IntrInfo[55:48]	Off (EasyTrigger group)
U8_Addr [39:32]	Off (EasyTrigger group)
U8_MT[2:0]	Off (EasyTrigger group)
U8_SysMgtCmd[7:0]	Off (EasyTrigger group)
U8_Addr[23:20]	Off (EasyTrigger group)
U8_MT[3:0]	Off (EasyTrigger group)
U8_Dest	Off (EasyTrigger group)
U8_RQEOI	Off (EasyTrigger group)
U8_IntrDest[7:0]	Off (EasyTrigger group)
U8_Vector[7:0}	Off (EasyTrigger group)
U8_IntrDest[23:8]	Off (EasyTrigger group)
U8_IntrDest[31:24]	Off (EasyTrigger group)
U8_ResponseData[1:0]	Off (EasyTrigger group)
U8_Response[1:0]	Off (EasyTrigger group)
U8_PostData[1:0]	Off (EasyTrigger group)
U8_PostCmd[1:0]	Off (EasyTrigger group)
U8_Isoc2	Off (EasyTrigger group)
U8_Diag	Off (EasyTrigger group)
U8_NonPostData[1:0]	Off (EasyTrigger group)
U8_NonPostCmd[1:0]	Off (EasyTrigger group)
U8_DataError	Off (EasyTrigger group)
U8_DestDev	Off (EasyTrigger group)
U8_DestFunc	Off (EasyTrigger group)
U8_DestBus	Off (EasyTrigger group)
U8_Type	Off (EasyTrigger group)
U8_Addr[39:29]	Off (EasyTrigger group)
D8_Cmd	Off (EasyTrigger group)
D8_SeqID[3:0]	Off (EasyTrigger group)
D8_PassPW	Off (EasyTrigger group)
D8_UnitID[4:0]	Off (EasyTrigger group)
D8_Count[3:0]	Off (EasyTrigger group)
D8_Compat	Off (EasyTrigger group)
D8_SrcTag[4:0]	Off (EasyTrigger group)
D8_Addr2[7:0]	Off (EasyTrigger group)

Table 3-1: HT and HT_Tek Channel groups (Cont.)

Group name	Display radix
D8_Addr3[7:0]	Off (EasyTrigger group)
D8_Addr[23:8]	Off (EasyTrigger group)
D8_Addr[39:24]	Off (EasyTrigger group)
D8_Addr[47:40]	Off (EasyTrigger group)
D8_Addr[63:48]	Off (EasyTrigger group)
D8_Isoc	Off (EasyTrigger group)
D8_Bridge	Off (EasyTrigger group)
D8_Error	Off (EasyTrigger group)
D8_NXA	Off (EasyTrigger group)
D8_IntrInfo[7:2]	Off (EasyTrigger group)
D8_IntrInfo[23:8]	Off (EasyTrigger group)
D8_IntrInfo[31:24]	Off (EasyTrigger group)
D8_IntrInfo[47:32]	Off (EasyTrigger group)
D8_IntrInfo[55:48]	Off (EasyTrigger group)
D8_Addr[39:32]	Off (EasyTrigger group)
D8_MT[2:0]	Off (EasyTrigger group)
D8_SysMgtCmd[7:0]	Off (EasyTrigger group)
D8_Addr[23:20]	Off (EasyTrigger group)
D8_MT[3:0]	Off (EasyTrigger group)
D8_Dest	Off (EasyTrigger group)
D8_RQEOI	Off (EasyTrigger group)
D8_IntrDest[7:0]	Off (EasyTrigger group)
D8_Vector[7:0]	Off (EasyTrigger group)
D8_IntrDest[23:8]	Off (EasyTrigger group)
D8_IntrDest[31:24]	Off (EasyTrigger group)
D8_ResponseData[1:0]	Off (EasyTrigger group)
D8_Response[1:0]	Off (EasyTrigger group)
D8_PostData[1:0]	Off (EasyTrigger group)
D8_PostCmd[1:0]	Off (EasyTrigger group)
D8_Isoc2	Off (EasyTrigger group)
D8_Diag	Off (EasyTrigger group)
D8_NonPostData[1:0]	Off (EasyTrigger group)
D8_NonPostCmd[1:0]	Off (EasyTrigger group)

Table 3-1: HT and HT_Tek Channel groups (Cont.)

Group name	Display radix
D8_DataError	Off (EasyTrigger group)
D8_DestDev	Off (EasyTrigger group)
D8_DestFunc	Off (EasyTrigger group)
D8_DestBus	Off (EasyTrigger group)
D8_Type	Off (EasyTrigger group)
D8_Addr[39:29]	Off (EasyTrigger group)

Symbol and Channel Assignment Tables

This section lists the symbol tables and channel assignment tables for disassembly and timing for each of the support packages.

Symbol Tables

The TMS855 HyperTransport support product includes symbol table files for some of the channel groups defined by the HT and HT_Tek support packages. Symbols may be used for triggering or display. The display radix of channel groups may be selected in the Column Properties menu on the logic analyzer.

Table 3–2 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the control symbol tables. The symbol table file for control channel group is HT_Ctrl.

Table 3-2: HT_Ctrl group symbol table definitions

	Control group value	
Symbol	**CTL**	**Description**
DATA	0	Data Packet
CTRL	1	Control Packet

Information on basic operations describes how to use symbolic values for triggering.

Channel Assignment Tables

Channel assignments shown in Table 3–3 through Table 3–16 use the following conventions:

- All signals are required by the support package, unless indicated otherwise.
- In Tables 3–4 through 3–9 and Tables 3–11 through 3–16, channels are shown starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- The prefixes U_ and D_ are used to distinguish the Upstream and Downstream signals.

HT Channel Group Assignments

Tables 3–3 through 3–9 show the channel assignments for the logic analyzer groups and the bus signal to which each channel connects.

Setup/Hold Calibration Groups

Table 3–3 shows the setup/hold calibration groups for HT support package.

Table 3-3: HT Setup/Hold calibration groups

Calibration group	HT support package channel name
$U_CTL	U_CTL
$U_CAD0	U_CAD0, U_CAD0_DM
$U_CAD1	U_CAD1, U_CAD1_DM
$U_CAD2	U_CAD2, U_CAD2_DM
$U_CAD3	U_CAD3, U_CAD3_DM
$U_CAD4	U_CAD4, U_CAD4_DM
$U_CAD5	U_CAD5, U_CAD5_DM
$U_CAD6	U_CAD6, U_CAD6_DM
$U_CAD7	U_CAD7, U_CAD7_DM
$U_CAD8	U_CAD8, U_CAD8_DM
$U_CAD9	U_CAD9, U_CAD9_DM
$U_CAD10	U_CAD10, U_CAD10_DM
$U_CAD11	U_CAD11, U_CAD11_DM
$U_CAD12	U_CAD12, U_CAD12_DM
$U_CAD13	U_CAD13, U_CAD13_DM
$U_CAD14	U_CAD14, U_CAD14_DM
$U_CAD15	U_CAD15, U_CAD15_DM
$D_CTL	D_CTL
$D_CAD0	D_CAD0, D_CAD0_DM
$D_CAD1	D_CAD1, D_CAD1_DM
$D_CAD2	D_CAD2, D_CAD2_DM
$D_CAD3	D_CAD3, D_CAD3_DM
$D_CAD4	D_CAD4, D_CAD4_DM
$D_CAD5	D_CAD5, D_CAD5_DM
$D_CAD6	D_CAD6, D_CAD6_DM
$D_CAD7	D_CAD7, D_CAD7_DM
$D_CAD8	D_CAD8, D_CAD8_DM
$D_CAD9	D_CAD9, D_CAD9_DM
$D_CAD10	D_CAD10, D_CAD10_DM

Table 3-3: HT Setup/Hold calibration groups (Cont.)

Calibration group	HT support package channel name
$D_CAD11	D_CAD11, D_CAD11_DM
$D_CAD12	D_CAD12, D_CAD12_DM
$D_CAD13	D_CAD13, D_CAD13_DM
$D_CAD14	D_CAD14, D_CAD14_DM
$D_CAD15	D_CAD15, D_CAD15_DM

Disassembly Groups for HT Support Package

Tables 3–4 through 3–9 list the disassembly groups for the HT support package.

HT Upstream channel group assignments. Tables 3–4 through 3–6 list the channel assignments for the Upstream bus and the bus signal to which each channel connects.

Table 3–4 lists the channel assignments for the U_CAD group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-4: U_CAD group assignments for HT support package

Section:Channel	HT support package channel name	Comments
C3:[7-0]	U_CAD[15-8]	Connected to target system
A3:[7-0]	U_CAD[7-0]	Connected to target system

Table 3–5 lists the channel assignments for the U_CAD_DM group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-5: U_CAD_DM group assignments for HT support package

Section:Channel	HT support package channel name	Comments
C1:[7-0]	U_CAD[15-8]_DM	Demuxed from C3
D3:[7-0]	U_CAD[7-0]_DM	Demuxed from A3

Table 3–6 lists the channel assignments for the U_Control group and the bus signal to which the channel connects. By default, this channel group is displayed in symbols.

Table 3-6: U_Control group assignments for HT support package

Section:Channel	HT support package channel name	Comments
Clk:0	U_CTL	Connected to target system

HT Downstream channel group assignments. Tables 3–7 through 3–9 list the channel assignments for the Downstream bus and the bus signal to which each channel connects.

Table 3–7 lists the channel assignments for the D_CAD group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-7: D_CAD group assignments for HT support package

Section:Channel	HT support package channel name	Comments
A1:[7-0]	D_CAD[15-8]	Connected to target system
E3:[7-0]	D_CAD[7-0]	Connected to target system

Table 3–8 lists the channel assignments for the D_CAD_DM group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-8: D_CAD_DM group assignments for HT support package

Section:Channel	HT support package channel name	Comments
D1:[7-0]	D_CAD[15-8]_DM	Demuxed from A1
E1:[7-0]	D_CAD[7-0]_DM	Demuxed from E3

Table 3–9 lists the channel assignments for the D_Control group and the bus signal to which the channel connects. By default, this channel group is displayed in symbols.

Table 3-9: D_Control group assignments for HT support package

Section:Channel	HT support package channel name	Comments
Qual:3	D_CTL	Connected to target system

HT_Tek Channel Group Assignments

Tables 3–10 through 3–16 show the channel assignments for the logic analyzer groups and the bus signal to which each channel connects.

Setup/Hold Calibration Groups

Table 3–10 shows the setup/hold calibration groups for HT_Tek support package.

Table 3-10: HT_Tek Setup/Hold calibration groups

Calibration group	HT_Tek support package channel name
$U_CTL	U_CTL
$U_CAD0	U_CAD0, U_CAD0_DM
$U_CAD1	U_CAD1, U_CAD1_DM
$U_CAD2	U_CAD2, U_CAD2_DM
$U_CAD3	U_CAD3, U_CAD3_DM
$U_CAD4	U_CAD4, U_CAD4_DM
$U_CAD5	U_CAD5, U_CAD5_DM
$U_CAD6	U_CAD6, U_CAD6_DM
$U_CAD7	U_CAD7, U_CAD7_DM
$U_CAD8	U_CAD8, U_CAD8_DM
$U_CAD9	U_CAD9, U_CAD9_DM
$U_CAD10	U_CAD10, U_CAD10_DM
$U_CAD11	U_CAD11, U_CAD11_DM
$U_CAD12	U_CAD12, U_CAD12_DM
$U_CAD13	U_CAD13, U_CAD13_DM
$U_CAD14	U_CAD14, U_CAD14_DM
$U_CAD15	U_CAD15, U_CAD15_DM
$D_CTL	D_CTL

Table 3-10: HT_Tek Setup/Hold calibration groups (Cont.)

Calibration group	HT_Tek support package channel name
$D_CAD0	D_CAD0, D_CAD0_DM
$D_CAD1	D_CAD1, D_CAD1_DM
$D_CAD2	D_CAD2, D_CAD2_DM
$D_CAD3	D_CAD3, D_CAD3_DM
$D_CAD4	D_CAD4, D_CAD4_DM
$D_CAD5	D_CAD5, D_CAD5_DM
$D_CAD6	D_CAD6, D_CAD6_DM
$D_CAD7	D_CAD7, D_CAD7_DM
$D_CAD8	D_CAD8, D_CAD8_DM
$D_CAD9	D_CAD9, D_CAD9_DM
$D_CAD10	D_CAD10, D_CAD10_DM
$D_CAD11	D_CAD11, D_CAD11_DM
$D_CAD12	D_CAD12, D_CAD12_DM
$D_CAD13	D_CAD13, D_CAD13_DM
$D_CAD14	D_CAD14, D_CAD14_DM
$D_CAD15	D_CAD15, D_CAD15_DM

Disassembly Groups for HT_Tek Support Package

Tables 3–11 through 3–16 lists the disassembly groups for HT_Tek support package.

HT_Tek Upstream channel group assignments. Tables 3–11 through 3–13 list the channel assignments for the Upstream bus and the bus signal to which each channel connects.

Table 3–11 lists the channel assignments for the U_CAD group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-11: U_CAD group assignments for HT_Tek support package

Section:Channel	HT_Tek support package channel name	Comments
C3:[7-0]	U_CAD[15-8]	Connected to target system
A3:[7-0]	U_CAD[7-0]	Connected to target system

Table 3–12 lists the channel assignments for the U_CAD_DM group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-12: U_CAD_DM group assignments for HT_Tek support package

Section:Channel	HT_Tek support package channel name	Comments
C1:[7-0]	U_CAD[15-8]_DM	Demuxed from C3
D3:[7-0]	U_CAD[7-0]_DM	Demuxed from A3

Table 3–13 lists the channel assignments for the U_Control group and the bus signal to which the channel connects. By default, this channel group is displayed in symbols.

Table 3-13: U_Control group assignments for HT_Tek support package

Section:Channel	HT_Tek support package channel name	Comments
Clk:3	U_CTL	Connected to target system

HT_Tek Downstream channel group assignments. Tables 3–14 through 3–16 list the channel assignments for the Downstream bus and the bus signal to which each channel connects.

Table 3–14 lists the channel assignments for the D_CAD group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-14: D_CAD group assignments for HT_Tek support package

Section:Channel	HT_Tek support package channel name	Comments
A1:[7-0]	D_CAD[15-8]	Connected to target system
E3:[7-0]	D_CAD[7-0]	Connected to target system

Table 3–15 lists the channel assignments for the D_CAD_DM group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-15: D_CAD_DM group assignments for HT_Tek support package

Section:Channel	HT_Tek support package channel name	Comments
D1:[7-0]	D_CAD[15-8]_DM	Demuxed from A1
E1:[7-0]	D_CAD[7-0]_DM	Demuxed from E3

Table 3–16 lists the channel assignments for the D_Control group and the bus signal to which the channel connects. By default, this channel group is displayed in symbols.

Table 3-16: D_Control group assignments for HT_Tek support package

Section:Channel	HT_Tek support package channel name	Comments
Qual:3	D_CTL	Connected to target system

Signal Source To Probe Connections

For design purposes, you may need to make connections between the Signal Source and the P6880 Logic Analyzer Probe. Refer to the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction* manual, Tektronix part number 071-1059-01, for more information on mechanical specifications.

Tables 3–17 through 3–34 list the Signal Source to P6880 probe pin connections.

Connections for HT and HT_Cal Support Packages

Tables 3–17 to 3–25 list the pin connections for the channel assignments for the HT support package.

Figure 3–1 shows P6880 differential probe land footprint for HT and HT_Cal support packages.

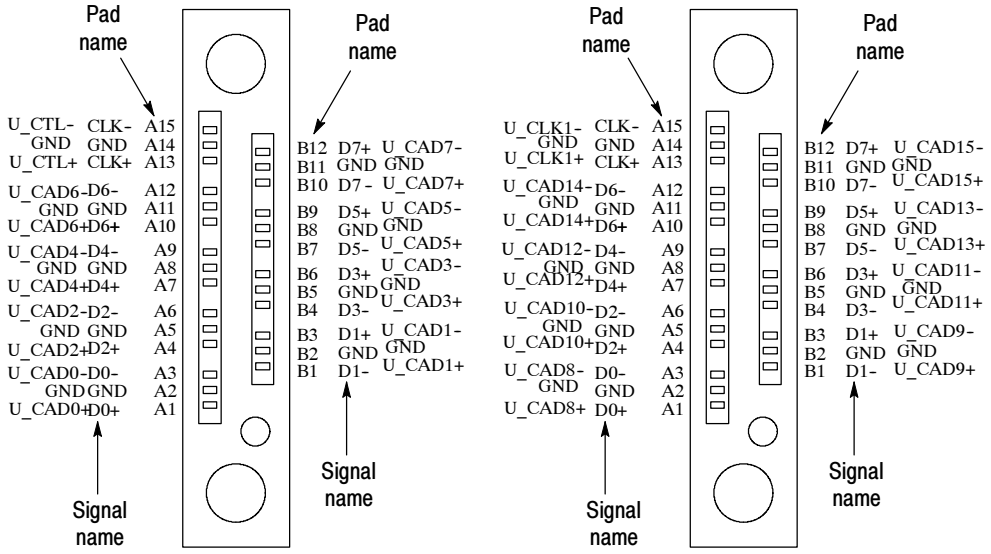
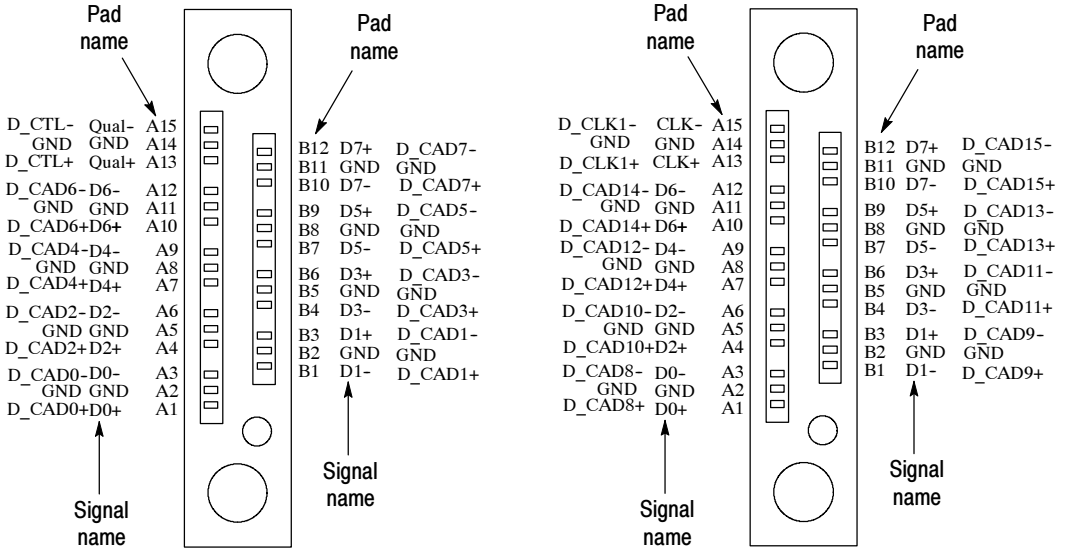


Figure 3–1: P6880 differential probe land footprint for HT and HT_Cal support packages



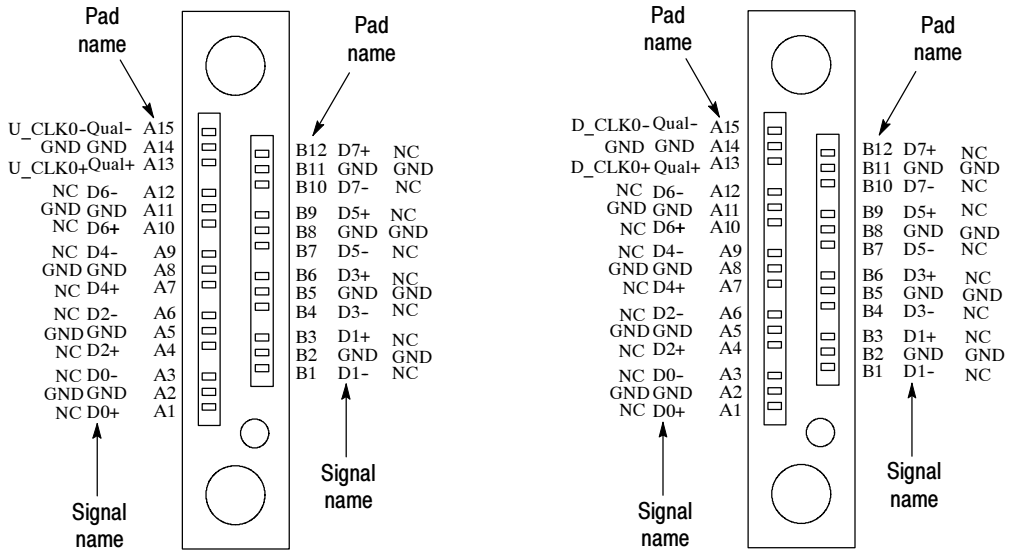


Figure 3-1: P6880 differential probe land footprint for HT and HT_Cal support packages (Cont)

***NOTE**. Within Figure 3-1, NC indicates NOT CONNECTED.*

Table 3–17 lists the pin connections for the clock and qualifier channel assignment.

***NOTE**. The HT support package channel assignments apply to the HT_Cal support package.*

Table 3-17: Clock and qualifier channel assignments for HT support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe number, probe head number	P6880 pad name	HT support package channel name
CK0	CK0-	Probe #3, Probe head 4	A15	U_CTL-
	CK0+	Probe #3, Probe head 4	A13	U_CTL+
CK1	CK1-	Probe #2, Probe head 4	A15	D_CLK1-
	CK1+	Probe #2, Probe head 4	A13	D_CLK1+
CK2	CK2-	Probe #2, Probe head 2	A15	NOT CONNECTED
	CK2+	Probe #2, Probe head 2	A13	NOT CONNECTED
CK3	CK3-	Probe #1, Probe head 4	A15	U_CLK1-
	CK3+	Probe #1, Probe head 4	A13	U_CLK1+
Q0	Q0-	Probe #3, Probe head 2	A15	U_CLK0-
	Q0+	Probe #3, Probe head 2	A13	U_CLK0+
Q1	Q1-	Probe #1, Probe head 2	A15	NOT CONNECTED

Table 3-17: Clock and qualifier channel assignments for HT support package (Cont.)

Logic analyzer acquisition channel	P6880 signal name	P6880 probe number, probe head number	P6880 pad name	HT support package channel name
	Q1+	Probe #1, Probe head 2	A13	NOT CONNECTED
Q2	Q2-	Probe #4, Probe head 2	A15	D_CLK0-
	Q2+	Probe #4, Probe head 2	A13	D_CLK0+
Q3	Q3-	Probe #4, Probe head 4	A15	D_CTL-
	Q3+	Probe #4, Probe head 4	A13	D_CTL+

Tables 3–18 through 3–21 list the pin connections for the Upstream channel assignments.

Table 3-18: A3 probe Upstream channel assignments for HT support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe 3 probe head 4	P6880 pad name	HT support package channel name
A3:7	Data7+	A3:7+	B12	U_CAD7-
	Data7-	A3:7-	B10	U_CAD7+
A3:6	Data6-	A3:6-	A12	U_CAD6-
	Data6+	A3:6+	A10	U_CAD6+
A3:5	Data5+	A3:5+	B9	U_CAD5-
	Data5-	A3:5-	B7	U_CAD5+
A3:4	Data4-	A3:4-	A9	U_CAD4-
	Data4+	A3:4+	A7	U_CAD4+
A3:3	Data3+	A3:3+	B6	U_CAD3-
	Data3-	A3:3-	B4	U_CAD3+
A3:2	Data2-	A3:2-	A6	U_CAD2-
	Data2+	A3:2+	A4	U_CAD2+
A3:1	Data1+	A3:1+	B3	U_CAD1-
	Data1-	A3:1-	B1	U_CAD1+
A3:0	Data0-	A3:0-	A3	U_CAD0-
	Data0+	A3:0+	A1	U_CAD0+

Table 3-19: D3 probe channel assignments for Upstream bus demuxed from A3 for HT support package

Logic analyzer acquisition channel	HT support package channel name
D3:7	U_CAD7_DM
D3:6	U_CAD6_DM
D3:5	U_CAD5_DM
D3:4	U_CAD4_DM
D3:3	U_CAD3_DM
D3:2	U_CAD2_DM
D3:1	U_CAD1_DM
D3:0	U_CAD0_DM

Table 3-20: C3 probe Upstream channel assignments for HT support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe 1 probe head 4	P6880 pad name	HT support package channel name
C3:7	Data7+	C3:7+	B12	U_CAD15-
	Data7-	C3:7-	B10	U_CAD15+
C3:6	Data6-	C3:6-	A12	U_CAD14-
	Data6+	C3:6+	A10	U_CAD14+
C3:5	Data5+	C3:5+	B9	U_CAD13-
	Data5-	C3:5-	B7	U_CAD13+
C3:4	Data4-	C3:4-	A9	U_CAD12-
	Data4+	C3:4+	A7	U_CAD12+
C3:3	Data3+	C3:3+	B6	U_CAD11-
	Data3-	C3:3-	B4	U_CAD11+
C3:2	Data2-	C3:2-	A6	U_CAD10-
	Data2+	C3:2+	A4	U_CAD10+
C3:1	Data1+	C3:1+	B3	U_CAD9-
	Data1-	C3:1-	B1	U_CAD9+
C3:0	Data0-	C3:0-	A3	U_CAD8-
	Data0+	C3:0+	A1	U_CAD8+

Table 3-21: C1 probe channel assignments for Upstream bus demuxed from C3 for HT support package

Logic analyzer acquisition channel	HT support package channel name
C1:7	U_CAD15_DM
C1:6	U_CAD14_DM
C1:5	U_CAD13_DM
C1:4	U_CAD12_DM
C1:3	U_CAD11_DM
C1:2	U_CAD10_DM
C1:1	U_CAD9_DM
C1:0	U_CAD8_DM

Tables 3–22 through 3–25 list the Downstream channel assignments for the HT support package.

Table 3-22: A1 probe Downstream channel assignments for HT support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe 2 probe head 4	P6880 pad name	HT support package channel name
A1:7	Data7+	A1:7+	B12	D_CAD15-
	Data7-	A1:7-	B10	D_CAD15+
A1:6	Data6-	A1:6-	A12	D_CAD14-
	Data6+	A1:6+	A10	D_CAD14+
A1:5	Data5+	A1:5+	B9	D_CAD13-
	Data5-	A1:5-	B7	D_CAD13+
A1:4	Data4-	A1:4-	A9	D_CAD12-
	Data4+	A1:4+	A7	D_CAD12+
A1:3	Data3+	A1:3+	B6	D_CAD11-
	Data3-	A1:3-	B4	D_CAD11+
A1:2	Data2-	A1:2-	A6	D_CAD10-
	Data2+	A1:2+	A4	D_CAD10+
A1:1	Data1+	A1:1+	B3	D_CAD9-
	Data1-	A1:1-	B1	D_CAD9+
A1:0	Data0-	A1:0-	A3	D_CAD8-
	Data0+	A1:0+	A1	D_CAD8+

Table 3-23: D1 probe channel assignments for Downstream bus demuxed from A1 for HT support package

Logic analyzer acquisition channel	HT support package channel name
D1:7	D_CAD15_DM
D1:6	D_CAD14_DM
D1:5	D_CAD13_DM
D1:4	D_CAD12_DM
D1:3	D_CAD11_DM
D1:2	D_CAD10_DM
D1:1	D_CAD9_DM
D1:0	D_CAD8_DM

Table 3-24: E3 probe Downstream channel assignments for HT support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe 4 probe head 4	P6880 pad name	HT support package channel name
E3:7	Data7+	E3:7+	B12	D_CAD7-
	Data7-	E3:7-	B10	D_CAD7+
E3:6	Data6-	E3:6-	A12	D_CAD6-
	Data6+	E3:6+	A10	D_CAD6+
E3:5	Data5+	E3:5+	B9	D_CAD5-
	Data5-	E3:5-	B7	D_CAD5+
E3:4	Data4-	E3:4-	A9	D_CAD4-
	Data4+	E3:4+	A7	D_CAD4+
E3:3	Data3+	E3:3+	B6	D_CAD3-
	Data3-	E3:3-	B4	D_CAD3+
E3:2	Data2-	E3:2-	A6	D_CAD2-
	Data2+	E3:2+	A4	D_CAD2+
E3:1	Data1+	E3:1+	B3	D_CAD1-
	Data1-	E3:1-	B1	D_CAD1+
E3:0	Data0-	E3:0-	A3	D_CAD0-
	Data0+	E3:0+	A1	D_CAD0+

Table 3-25: E1 probe channel assignments for Downstream bus demuxed from E3 for HT support package

Logic analyzer acquisition channel	HT support package channel name
E1:7	D_CAD7_DM
E1:6	D_CAD6_DM
E1:5	D_CAD5_DM
E1:4	D_CAD4_DM
E1:3	D_CAD3_DM
E1:2	D_CAD2_DM
E1:1	D_CAD1_DM
E1:0	D_CAD0_DM

P6880 probe channels not connected. A2, A0, D2, D0, C2, C0, E2, and E0 probe channels are not connected and not used.

Demuxed P6880 probe channels. D3, D1, C1, and E1 probe channels are internally connected and should not be used.

Connections for HT_Tek and HT_Tek_Cal Support Packages

Tables 3-26 through 3-34 list pin connections for the channel assignments for the HT_Tek support package.

Figure 3-2 shows P6880 differential probe land footprint for HT_Tek and HT_Tek_Cal support packages.

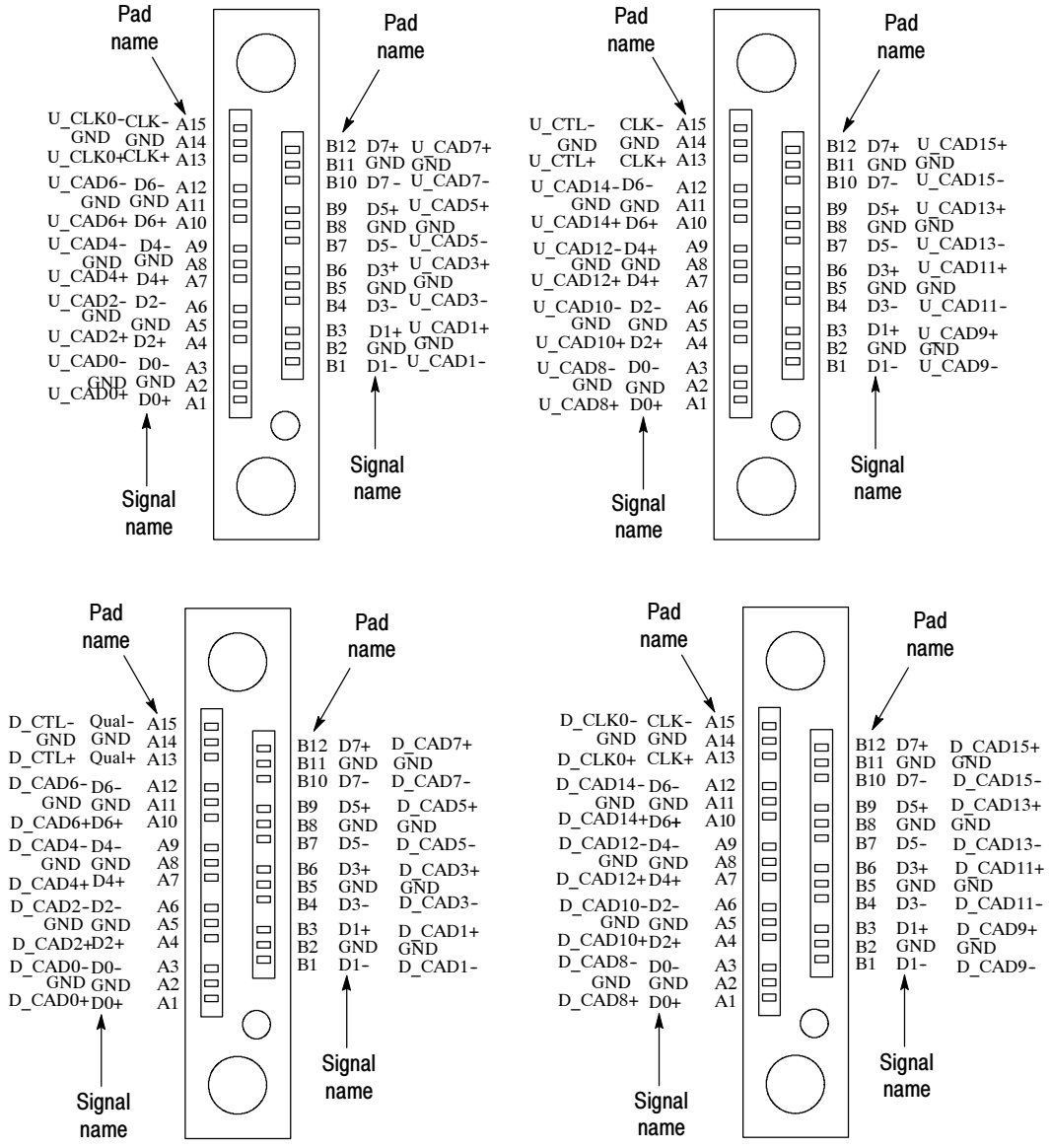


Figure 3-2: P6880 differential probe land footprint for HT_Tek and HT_Tek_Cal support packages

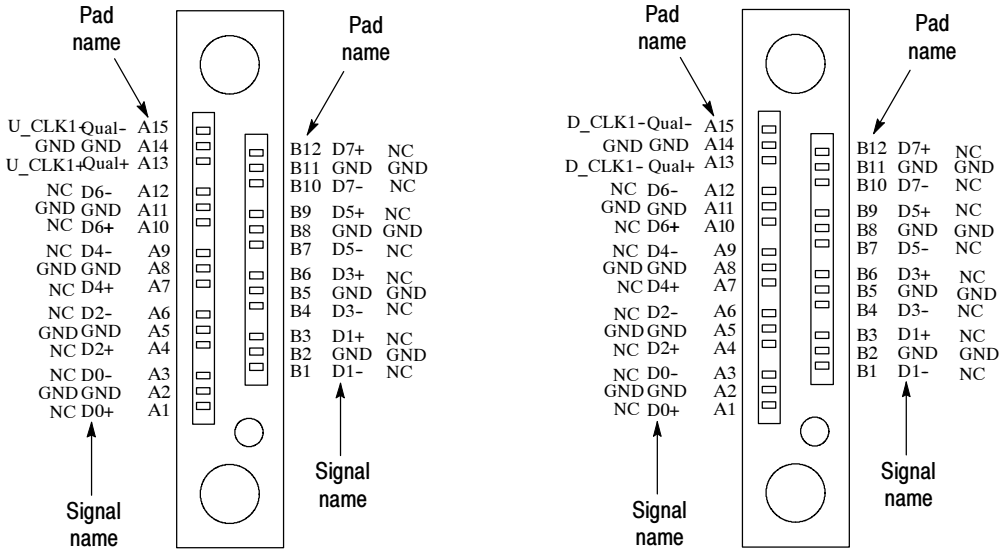


Figure 3-3: P6880 differential probe land footprint for HT_Tek and HT_Tek_Cal support packages

***NOTE**. The HT_Tek support package channel assignments apply to the HT_Tek_Cal support package.*

Table 3-26 lists the pin connections for the clock and qualifier channels.

Table 3-26: Clock and qualifier channel assignments for HT_Tek support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe number, probe head number	P6880 pad name	HT_Tek support package channel name
CK0	CK0-	Probe #3, Probe head 4	A15	U_CLK0-
	CK0+	Probe #3, Probe head 4	A13	U_CLK0+
CK1	CK1-	Probe #2, Probe head 4	A15	D_CLK0-
	CK1+	Probe #2, Probe head 4	A13	D_CLK0+
CK2	CK2-	Probe #2, Probe head 2	A15	NOT CONNECTED
	CK2+	Probe #2, Probe head 2	A13	NOT CONNECTED
CK3	CK3-	Probe #1, Probe head 4	A15	U_CTL-
	CK3+	Probe #1, Probe head 4	A13	U_CTL+
Q0	Q0-	Probe #3, Probe head 2	A15	D_CLK1-
	Q0+	Probe #3, Probe head 2	A13	D_CLK1+
Q1	Q1-	Probe #1, Probe head 2	A15	U_CLK1-
	Q1+	Probe #1, Probe head 2	A13	U_CLK1+
Q2	Q2-	Probe #4, Probe head 2	A15	NOT CONNECTED

Table 3-26: Clock and qualifier channel assignments for HT_Tek support package (Cont.)

Logic analyzer acquisition channel	P6880 signal name	P6880 probe number, probe head number	P6880 pad name	HT_Tek support package channel name
	Q2+	Probe #4, Probe head 2	A13	NOT CONNECTED
Q3	Q3-	Probe #4, Probe head 4	A15	D_CTL-
	Q3+	Probe #4, Probe head 4	A13	D_CTL+

Tables 3–27 through 3–30 list the pin connections for the Upstream channel assignments.

Table 3-27: A3 probe Upstream channel assignments for HT_Tek support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe 3 probe head4	P6880 pad name	HT_Tek support package channel name
A3:7	Data7+	A3:7+	B12	U_CAD7+
	Data7-	A3:7-	B10	U_CAD7-
A3:6	Data6-	A3:6-	A12	U_CAD6-
	Data6+	A3:6+	A10	U_CAD6+
A3:5	Data5+	A3:5+	B9	U_CAD5+
	Data5-	A3:5-	B7	U_CAD5-
A3:4	Data4-	A3:4-	A9	U_CAD4-
	Data4+	A3:4+	A7	U_CAD4+
A3:3	Data3+	A3:3+	B6	U_CAD3+
	Data3-	A3:3-	B4	U_CAD3-
A3:2	Data2-	A3:2-	A6	U_CAD2-
	Data2+	A3:2+	A4	U_CAD2+
A3:1	Data1+	A3:1+	B3	U_CAD1+
	Data1-	A3:1-	B1	U_CAD1-
A3:0	Data0-	A3:0-	A3	U_CAD0-
	Data0+	A3:0+	A1	U_CAD0+

Table 3-28: D3 probe channel assignments for Upstream bus demuxed from A3 for HT_Tek support package

Logic analyzer acquisition channel	HT_Tek support package channel name
D3:7	U_CAD7_DM
D3:6	U_CAD6_DM
D3:5	U_CAD5_DM
D3:4	U_CAD4_DM
D3:3	U_CAD3_DM
D3:2	U_CAD2_DM
D3:1	U_CAD1_DM
D3:0	U_CAD0_DM

Table 3-29: C3 probe Upstream channel assignments for HT_Tek support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe 1 probe head 4	P6880 pad name	HT_Tek support package channel name
C3:7	Data7+	C3:7+	B12	U_CAD15+
	Data7-	C3:7-	B10	U_CAD15-
C3:6	Data6-	C3:6-	A12	U_CAD14-
	Data6+	C3:6+	A10	U_CAD14+
C3:5	Data5+	C3:5+	B9	U_CAD13+
	Data5-	C3:5-	B7	U_CAD13-
C3:4	Data4-	C3:4-	A9	U_CAD12-
	Data4+	C3:4+	A7	U_CAD12+
C3:3	Data3+	C3:3+	B6	U_CAD11+
	Data3-	C3:3-	B4	U_CAD11-
C3:2	Data2-	C3:2-	A6	U_CAD10-
	Data2+	C3:2+	A4	U_CAD10+
C3:1	Data1+	C3:1+	B3	U_CAD9+
	Data1-	C3:1-	B1	U_CAD9-
C3:0	Data0-	C3:0-	A3	U_CAD8-
	Data0+	C3:0+	A1	U_CAD8+

Table 3-30: C1 probe channel assignments for Upstream bus demuxed from C3 for HT_Tek support package

Logic analyzer acquisition channel	HT_Tek support package channel name
C1:7	U_CAD15_DM
C1:6	U_CAD14_DM
C1:5	U_CAD13_DM
C1:4	U_CAD12_DM
C1:3	U_CAD11_DM
C1:2	U_CAD10_DM
C1:1	U_CAD9_DM
C1:0	U_CAD8_DM

Tables 3–31 through 3–34 list the Downstream channel assignments for the HT16 support package.

Table 3-31: A1 probe Downstream channel assignments for HT_Tek support package

Logic analyzer acquisition channel	P6880 signal name	P6880 probe 2 probe head 4	P6880 pad name	HT_Tek support package channel name
A1:7	Data7+	A1:7+	B12	D_CAD15+
	Data7-	A1:7-	B10	D_CAD15-
A1:6	Data6-	A1:6-	A12	D_CAD14-
	Data6+	A1:6+	A10	D_CAD14+
A1:5	Data5+	A1:5+	B9	D_CAD13+
	Data5-	A1:5-	B7	D_CAD13-
A1:4	Data4-	A1:4-	A9	D_CAD12-
	Data4+	A1:4+	A7	D_CAD12+
A1:3	Data3+	A1:3+	B6	D_CAD11+
	Data3-	A1:3-	B4	D_CAD11-
A1:2	Data2-	A1:2-	A6	D_CAD10-
	Data2+	A1:2+	A4	D_CAD10+
A1:1	Data1+	A1:1+	B3	D_CAD9+
	Data1-	A1:1-	B1	D_CAD9-
A1:0	Data0-	A1:0-	A3	D_CAD8-
	Data0+	A1:0+	A1	D_CAD8+

Table 3-32: D1 probe channel assignments for Downstream bus demuxed from A1 for HT_Tek support package

Logic analyzer acquisition channel	HT_Tek support package channel name
D1:7	D_CAD15_DM
D1:6	D_CAD14_DM
D1:5	D_CAD13_DM
D1:4	D_CAD12_DM
D1:3	D_CAD11_DM
D1:2	D_CAD10_DM
D1:1	D_CAD9_DM
D1:0	D_CAD8_DM

Table 3-33: E3 probe Downstream channel assignments for HT_Tek support package

Logic Analyzer acquisition channel	P6880 signal name	P6880 probe 4 probe head 4	P6880 pad name	HT_Tek support package channel name
E3:7	Data7+	E3:7+	B12	D_CAD7+
	Data7-	E3:7-	B10	D_CAD7-
E3:6	Data6-	E3:6-	A12	D_CAD6-
	Data6+	E3:6+	A10	D_CAD6+
E3:5	Data5+	E3:5+	B9	D_CAD5+
	Data5-	E3:5-	B7	D_CAD5-
E3:4	Data4-	E3:4-	A9	D_CAD4-
	Data4+	E3:4+	A7	D_CAD4+
E3:3	Data3+	E3:3+	B6	D_CAD3+
	Data3-	E3:3-	B4	D_CAD3-
E3:2	Data2-	E3:2-	A6	D_CAD2-
	Data2+	E3:2+	A4	D_CAD2+
E3:1	Data1+	E3:1+	B3	D_CAD1+
	Data1-	E3:1-	B1	D_CAD1-
E3:0	Data0-	E3:0-	A3	D_CAD0-
	Data0+	E3:0+	A1	D_CAD0+

Table 3-34: E1 probe channel assignments for Downstream bus demuxed from E3 for HT_Tek support package

Logic analyzer acquisition channel	HT_Tek support package channel name
E1:7	D_CAD7_DM
E1:6	D_CAD6_DM
E1:5	D_CAD5_DM
E1:4	D_CAD4_DM
E1:3	D_CAD3_DM
E1:2	D_CAD2_DM
E1:1	D_CAD1_DM
E1:0	D_CAD0_DM

P6880 probe channels not connected. A2, A0, D2, D0, C2, C0, E2, and E0 probe channels are not connected and not used.

Demuxed P6880 probe channels. D3, D1, C1, and E1 probe channels are internally connected and should not be used.

Signal Acquisition

This section contains timing diagrams that show how to acquire the data from the target system using the TMS855 HyperTransport bus support product.

Signal Acquisition in HT and HT_Tek Support Packages

The TMS855 HyperTransport bus support product takes advantage of the two way demux feature of the logic analyzer hardware to acquire the HyperTransport link up to 900 Mb/s provided that the data valid window is 750 ps. The data on the HyperTransport link is transmitted at both edges of the clock (rising and falling). The TLA7Axx modules can support speeds up to 450 MHz. Depending on the custom clocking options selected, the HT and HT_Tek support packages use U_CLK0, U_CLK1, D_CLK0 or D_CLK1 signals as the source clock domain. Eight custom clocking options are displayed as follows:

- 1: Upstream UCLK0
- 2: Upstream UCLK0 inverted
- 3: Upstream UCLK1
- 4: Upstream UCLK1 inverted
- 5: Downstream DCLK0
- 6: Downstream DCLK0 inverted
- 7: Downstream DCLK1
- 8: Downstream DCLK1 inverted

Table 3-35 lists the figures corresponding to various combinations of acquisition modes and clocking options.

Table 3-35: Reference of figures corresponding to combinations of acquisition modes and clocking options

Source clock domain	Buswidth	Figure	Acquisition mode
U_CLK0 D_CLK0	8-bit	3-4	Upstream or Downstream only.
Inverted U_CLK0 Inverted D_CLK0	8-bit	3-5	Upstream or Downstream only.
U_CLK0 D_CLK0	8-bit	3-6	Upstream and Downstream with no skew between Upstream and Downstream clocks.

Table 3-35: Reference of figures corresponding to combinations of acquisition modes and clocking options (Cont.)

Source clock domain	Buswidth	Figure	Acquisition mode
U_CLK0 D_CLK0	8-bit	3-7	Upstream and Downstream with some skew between Upstream and Downstream clocks.
Inverted U_CLK0 Inverted D_CLK0	8-bit	3-6	Upstream and Downstream with no skew between the Upstream and Downstream clocks
Inverted U_CLK0 Inverted D_CLK0	8-bit	3-7	Upstream and Downstream with some skew between upstream and Downstream clocks.
U_CLK0 D_CLK0	8-bit	3-8	Upstream and Downstream with Upstream and Downstream clocks 180 degrees out of phase.
Inverted U_CLK0 Inverted D_CLK0	8-bit	3-8	Upstream and Downstream with Upstream and Downstream clocks 180 degrees out of phase.

NOTE. You can use U_CLK1 or D_CLK1 signals in place of U_CLK0 or D_CLK0 signals for 16-bit buses.

Figure 3-4 shows Upstream or Downstream data being acquired using their respective clocks.

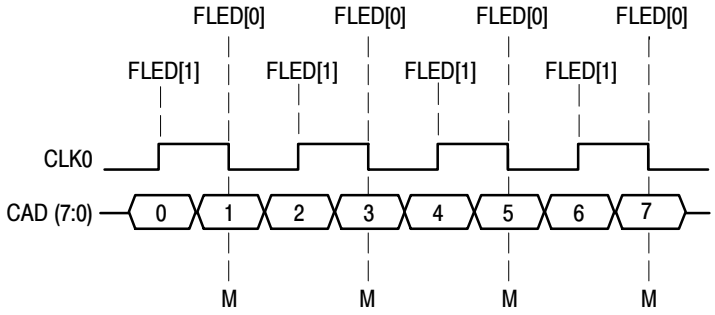


Figure 3-4: Timing diagram for Upstream or Downstream bus.

Data transmission starts on the rising edge of the clock after reset. The control and data packets are all 32 bits or multiples of 32 bits; therefore, the start of every packet is a rising edge.

The 2x demux feature is used to pair the data at the rising edge with the data at the falling edge, the paired data appears in the following sequence:

- data:0 and data:1
- data:2 and data:3
- data:4 and data:5 and so on.

Figure 3-5 shows Upstream or Downstream data being acquired using the inverted clocks.

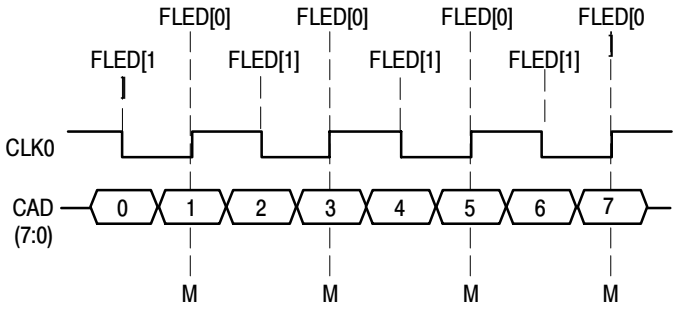


Figure 3-5: Timing diagram for Upstream and Downstream bus with Clock Inverted.

Data transmission starts on the falling edge of the clock after reset. The control and data packets are all 32 bits or multiples of 32 bits; therefore, the start of every packet is a falling edge.

The 2x demux feature is used to pair the data at the falling edge with the data at the rising edge, the paired data appears in the following sequence:

- data:0 and data:1
- data:2 and data:3
- data:4 and data:5 and so on.

Figure 3-6 shows both Upstream and Downstream buses being acquired using one of the clocks.

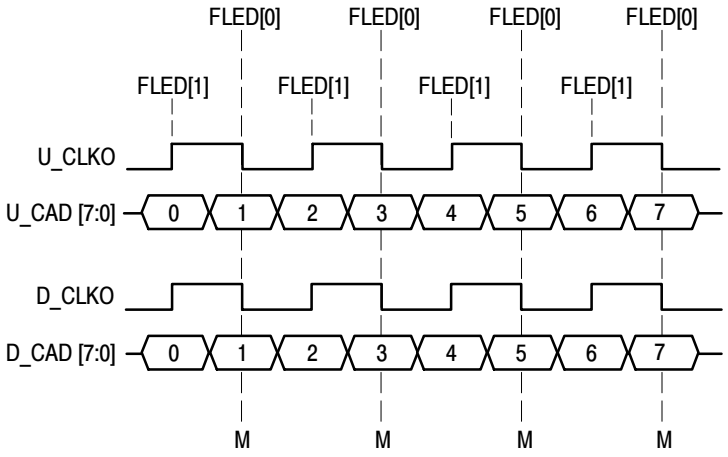


Figure 3-6: Timing diagram for Upstream and Downstream bus

It is assumed that there is no skew in the Upstream and Downstream clock signals and that both the clocks are running at the same speed (and derived from the same crystal), the paired data appears in sequence as follows for both Upstream and Downstream:

- data:0 and data:1
- data:2 and data:3
- data:4 and data:5 and so on.

Figure 3-7 shows both the Upstream and the Downstream buses being acquired when there is a skew between the Upstream and Downstream clock signals. You must adjust the setup/hold window such that Downstream data:0 (D_CAD) is acquired at the rising edge of U_CLK0 signal, and Downstream data:1 (D_CAD) is acquired at the falling edge of U_CLK0 signal.

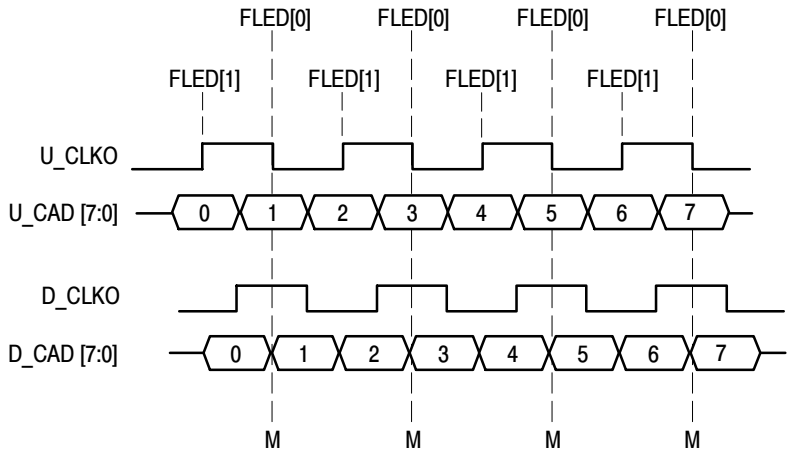


Figure 3-7: Timing diagram for Upstream and Downstream bus with skew

When you run the SHAnalyzer application with the U_CLK0 as the source clock domain, the application examines the Downstream data stability with respect to U_CLK0 signal. The suggested window is the nearest stable window that the SHAnalyzer application can find with respect to the rising edge of U_CLK0 signal for acquiring Downstream data:0, similarly for the falling edge data.

If you use inverted clocks the operation is similar except that the data at the falling edge is paired with data at rising edge.

Figure 3-8 shows both Upstream and Downstream buses being acquired when there is a phase shift of180 degrees between the upstream and downstream clocks.

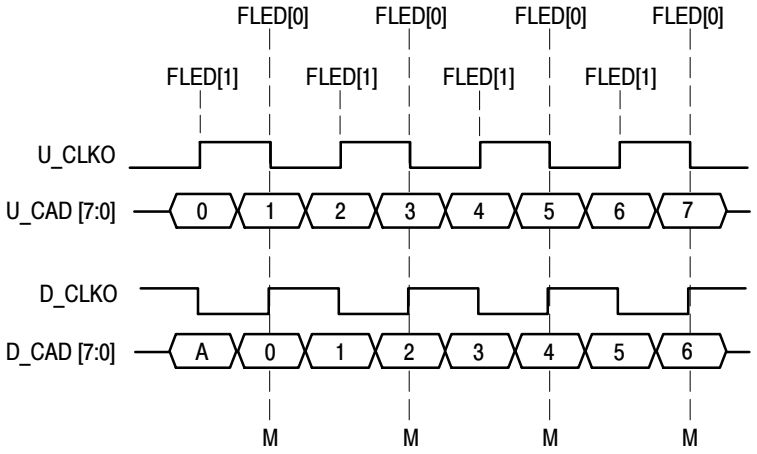


Figure 3-8: Timing diagram for Upstream and Downstream with 180 degree phase shift

When you run the SHAnalyzer application with U_CLK0 signal as source clock domain, the application examines the Downstream data stability with respect to U_CLK0 signal. The suggested window is the nearest stable window that the application can find with respect to rising edge of U_CLK0, it is Downstream data:A (not data:0). Similarly for the falling edge, it is Downstream data:0.

The correct pairing (rising and falling) for Upstream data is:

- data:0 and data:1,
- data:2 and data:3,
- data:4, data:5 and so on.

The correct pairing (rising and falling) for the Downstream data is:

- data:0 and data:1,
- data:2, data:3 and so on.

But the falling and rising pairing that appears for Downstream data is data:A and data:0, data:1 and data:2, data:3 and data:4 and so on. Which is incorrect.

When the pairing is incorrect, the disassembler cannot identify the CRC packets; therefore, the disassembler cannot synchronize its self and displays the message:

“*** Insufficient data to disassemble *** ”

Shifting the Setup/Hold window by half a clock can rectify the incorrect pairing.

***NOTE**. If the inverted clocks are used the operation is similar except that the data at falling edge is paired with data at rising edge.*

Table 3-36 lists the sample points in the HT and HT_Tek support packages.

Table 3-36: Sample points in the HT and HT_Tek support packages

Master point	Signals
M	U_CLK0, U_CAD[7:0], U_CLK1, U_CAD[15:8], U_CTL. D_CLK0, D_CAD[7:0], D_CLK1, D_CAD[15:8], D_CTL.

Specifications

Specifications

This section contains the specifications for the TMS855 HyperTransport bus support product.

Specifications Table

Table 4–1 lists the electrical requirements that the target system must produce for the TMS855 HyperTransport bus support product to acquire correct data.

Table 4–1: Electrical specifications

Characteristics	Requirements
Target system clock rate	
TMS855 specified clock rate for state acquisition supports for HT and HT_Tek support packages	Maximum 450 MHz[1]
Minimum data valid window required for state acquisition (measured at threshold)	750 ps (typical)

[1] **This is the specification at the time of printing. Contact your Tektronix representative for current information on the fastest bus supported.**

Replaceable Parts List

Replaceable Parts List

This section contains a list of the replaceable components and modules for the TMS855 HyperTransport bus support product. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

The tabular information in the *Replaceable Parts List* is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part..
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX, INC.	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR, 97077-0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-1170-XX			1	MANUAL,TECH INSTRUCTION,TMS855; HyperTransport Bus Support	80009	071-1170-XX

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